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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,382	02/16/2000	Roy R. Faget	10001840-1	6474

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EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	10

DATE MAILED: 04/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Applicati n No. 09/505,382	Applicant(s) FAGET, ROY R.
	Examiner Chat C. Do	Art Unit 2124

--The MAILING DATE of this c mmunication appears on the c ver sh et with the correspondence address --

THE REPLY FILED 31 March 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-20*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

CHUONG DINH NGO
PRIMARY EXAMINER

Continuation of 5. does NOT place the application in condition for allowance because: Tanihira et al. (U.S. 5,553,010) clearly disclose a data shift circuit in Figure 6 comprising a plurality of logic gates (Logic I 110-113 & 15, Logic II 120-123 & 16, Logic III 130-133 & 17, Logic IV 140-143 & 18) for receiving data input (Din0-Din3) and control signals (S0-S3 and 19) wherein each data input uses a single transistor (each input goes to a single transistor of an AND gate); and a plurality of shared data lines (Din0-Din2 bus) connecting logic gates. The shared data lines (Din0-Din2 bus) interfacing through a transistor on each of the logic gates (above Logic I-IV gates) to provide a portion of the data inputs (Din0-Din2) for each of the logic gates by connecting data inputs among the plurality of logic gates. The logic gates shift data received at the data inputs by one data bits based upon the control signals (S0-S3 and 19) and the connections of the shared data lines (Din0-Din2 bus) wherein each of the logic gates receives one data input (Din 3) using the single transistor for the data input and receives other data inputs (Din0-Din2) from the plurality of shared data lines (Din0-Din2 bus). In addition, Tanihira et al. disclose the logic gate in Figure 6 shift data received at the data inputs (Din) based upon the control signals (S0-S3) and connections of the shared data. Tanihira et al. disclose the first and second control signals are enable to shift either left/right (output data) .